IN THE CLAIMS:

Rewrite the pending claims and add new claims as follows:

- 1. (Currently Amended) An electronic silicon device comprising:
 - a silicon substrate comprising a planar surface;
- a trench disposed in said planar surface of said silicon substrate, said trench comprising a wall and a bottom;
- a silicon dioxide layer disposed on the bottom of said trench and also on a first portion of said wall, said layer being terminated at a distance D below said planar surface of said silicon device;
- a polysilicon fill disposed on the surface of said silicon dioxide layer and on a second portion of said wall; and
- a metallization disposed on the planar surface of said silicon substrate and an upper surface of said polysilicon fill.
- 2. (Currently Amended) The electronic silicon device of claim 1, wherein said polysilicon fill comprises an upper surface that is within a distance D from said planar surface of said silicon substrate the upper surface of said polysilicon fill is approximately level with or above said planar surface of said silicon substrate.
- 3. (Original) The electronic silicon device of claim 1, further comprising a junction field effect transistor (JFET).
- 4. (Canceled)
- 5. (Original) The electronic silicon device of claim 1, further comprising an integrated circuit.
- 6. (Original) The electronic silicon device of claim 1, wherein said trench is disposed above a gate.
- 7. (Original) The electronic silicon device of claim 1, wherein said trench is disposed adjacent to a source.

- 8. (Original) The electronic silicon device of claim 1, wherein said silicon dioxide layer is between 100 angstroms and 3000 angstroms in thickness.
- 9. (Original) The electronic silicon device of claim 1, wherein said silicon dioxide layer is thermally grown.
- 10. (Original) The electronic silicon device of claim 1, wherein said silicon dioxide layer is deposited.

11-20 (Cancelled)

- 21. (Currently Amended) A semiconductor device comprising:
 - a silicon substrate;
 - a trench disposed in said silicon substrate, said trench comprising a wall and a bottom;
- a silicon dioxide layer disposed on the bottom of said trench and also on a first portion of said wall, said layer being terminated below an original surface of said silicon substrate;
- a polysilicon fill disposed on the surface of said silicon dioxide layer and on a second

portion of said wall; and

a metallization disposed on the original surface of said silicon substrate and an upper surface of said polysilicon fill.

- 22. (Previously presented) The semiconductor device of claim 21, wherein said polysilicon fill comprises an upper surface that is disposed between a top surface of said silicon dioxide layer and said original surface of said silicon substrate.
- 23. (Previously presented) The semiconductor device of claim 21, further comprising a junction field effect transistor (JFET).
- 24. (Canceled)
- 25. (Previously presented) The semiconductor device of claim 21, further comprising an integrated circuit.
- 26. (Previously presented) The semiconductor device of claim 21, wherein said trench is disposed above a gate structure.

- 27. (Previously presented) The semiconductor device of claim 21, wherein said trench is disposed adjacent to a source structure.
- 28. (Previously presented) The semiconductor device of claim 21, wherein said silicon dioxide layer is between 100 angstroms and 1000 angstroms in thickness.
- 29. (Previously presented) The semiconductor device of claim 21, wherein said silicon dioxide layer is thermally grown.
- 30. (Previously presented) The semiconductor device of claim 21, wherein said silicon dioxide layer is deposited.
- 31. (Previously presented) The electronic silicon device of claim 1, wherein the polysilicon fill disposed on the second portion of said wall is in contact with a doped region of said silicon substrate.
- 32. (Previously presented) The semiconductor device of claim 21, wherein the polysilicon fill disposed on the second portion of said wall is in contact with a doped region of said silicon substrate.